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CLASS-D POWER AMPLIFIER CAPABLE OF ELIMINATING EXCESSIVE RESPONSE PHENOMENON WHEN RETURNING TO A STEADY STATE FROM AN ABNORMAL STATE AND AN AMPLIFICATION METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to Korean Patent Application No. 2003-29624, filed on 10 May 2003 at the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to a power amplifier, and more particularly, to a class-D power amplifier for use as an audio amplifier, and an amplification method thereof.

2. Discussion of the Related Art

In the past, class-A, class-B, and class-AB power amplifiers, which perform linear amplification, have been used as mainstream audio power amplifiers. Recently, however, there has been research conducted on class-D power amplifiers, which perform amplification by utilizing switching operations based on pulse width modulation (PWM). Research has shown that class-D power amplifiers have poor linearity and superior power efficiency as compared to class-A, class-B, and class-AB power amplifiers, which have superior linearity and poor power efficiency.

Switching operations based on PWM in class-D power amplifiers result in harmonic distortion caused by high-frequency components and oscillations. To overcome such harmonic distortion, negative feedback has been used in class-D power amplifiers. In addition, because an audio power amplifier is driven with high current, it has additional functions for protecting components in an initial state or an abnormal state, such as an over-current condition or a power-failure state. U.S. Patent Nos. 5,805,020 and 6,420,930 disclose exemplary class-D power amplifiers using negative feedback.

In a conventional class-D power amplifier using negative feedback, a predetermined switch is opened in the initial state or the abnormal state and negative feedback looping is blocked, thereby preventing over-current from flowing through the load side, such as a speaker. Here, an integral control circuit or proportional integral control circuit is input with a finite error signal and reaches a saturation state. In the saturation state, the predetermined switch is closed and there is a negative feedback loop so that the class-D power amplifier enters a steady state after the initial state or exits from an abnormal state. Then, because the integral control circuit or proportional integral control circuit is in the saturation state, an output signal exhibits an unstable excessive response phenomenon while the class-D power amplifier reaches the steady state.

To remedy the unstable excessive response phenomenon, the conventional class-D power amplifier includes an output-blocking switch before the load side, which outputs the output signal to the load side after the excessive response phenomenon is removed, and then the class-D power amplifier reaches the steady state. The rated power of the output-blocking switch corresponds to power consumed by the entire amplifying system in the steady state, which results in high power consumption by the conventional class-D power amplifier.

SUMMARY OF THE INVENTION

The present invention provides a class-D power amplifier, which prevents an excessive response phenomenon from occurring when the amplifier returns to a steady state from an abnormal state without using a high-capacity output-blocking switch. The present invention also provides an amplification method for a class-D power amplifier, which prevents an excessive response phenomenon from occurring when the amplifier returns to a steady state from an abnormal state without using a high-capacity output-blocking switch.

According to one aspect of the present invention, there is provided a class-D power amplifier comprising a summing circuit, an integral control circuit, a feedback control circuit, a switching circuit, a sub-negative feedback circuit, a controlled circuit, and a steady-state negative feedback circuit.

The summing circuit outputs an error signal by summing an input signal with one of a first negative feedback signal and a second negative feedback signal. The

integral control circuit outputs an integral signal by integrating the error signal. The feedback control circuit generates and outputs a switching control signal whose logic state changes according to the logic state of an abnormal state detecting signal generated in response to a monitoring signal.

The switching circuit switched the integral signal to one of a sub-loop and a steady-state loop in response to the switching control signal. The sub-negative feedback circuit receives and processes the integral signal and generates and outputs a sub-negative feedback signal as the first negative feedback signal. The controlled circuit modulates the integral signal into a pulse width modulation (PWM) signal and outputs an output signal. The steady-state negative feedback circuit receives and processes the output signal from the controlled circuit and generates and outputs a steady-state negative feedback signal as the second negative feedback signal.

The controlled circuit comprises a PWM circuit, a switching amplification circuit, and a low-pass filter (LPF) circuit. The PWM circuit modulates the integral signal output to the steady-state loop into the PWM signal using a sawtooth wave signal and outputs a PWM signal. The switching amplification circuit outputs an amplified signal according to the PWM signal. The low-pass filter (LPF) circuit receives the amplified signal and outputs a low-pass filtered signal generated by performing low-pass filtering on the amplified signal.

The feedback control circuit comprises a sawtooth wave signal generator, a slope detector, an abnormal state detector, and a feedback decider. The sawtooth wave signal generator generates and outputs the sawtooth wave signal. The slope detector generates and outputs a signal representing the slope of the sawtooth wave signal, where the logic state of the signal representing the slope of the sawtooth wave signal changes according the slope of the sawtooth wave signal. In response to the monitoring signal, the abnormal state detector generates and outputs the abnormal state detection signal that has different logic states when the monitoring signal is greater than an upper threshold and less than a lower threshold. The feedback decider generates the switching control signal whose logic state changes according to the logic state of the abnormal state detection signal and outputs the switching control signal.

When the integral signal is switched from the sub-loop to the steady-state loop, the logic state of the switching control signal changes in synchronization with the signal representing the slope of the sawtooth wave signal. The monitoring signal is

greater than the upper threshold in the abnormal state and the sub-negative feedback signal generated in the abnormal state prevents the integral signal from becoming saturated.

The PWM signal maintains a pulse width that is half the pulse width of the PWM signal in a steady-state when the input signal is a fog signal, after the logic state of the switching control signal changes when the integral signal is switched from the sub-loop to the steady-state loop. The pulse width of the PWM signal is the same pulse width as the pulse width of the switching control signal when the integral signal is switched from the sub-loop to the steady-state loop.

According to another aspect of the present invention, there is provided an amplification method of a class-D power amplifier. The amplification method comprises: (a) outputting an error signal by summing an input signal with one of a first negative feedback signal and a second negative feedback signal, (b) outputting an integral signal by integrating the error signal, (c) generating and outputting a switching control signal whose logic state changes according to the logic state of an abnormal state detection signal generated in response to a monitoring signal, (d) switching the integral signal to one of a sub-loop and a steady-state loop in response to the logic state of the switching control signal, (e) receiving and processing the integral signal and generating and outputting a sub-negative feedback signal as the first negative feedback signal, (f) receiving and modulating the integral signal into a PWM signal and outputting an output signal, and (g) processing the output signal and generating and outputting a steady-state negative feedback signal as the second negative feedback signal.

Step (f) comprises modulating the integral signal output to the steady-state loop into the PWM signal using a sawtooth wave signal and outputting the PWM signal, outputting an amplified signal according to the PWM signal, and outputting the output signal generated by performing low-pass filtering on the amplified signal.

Step (c) comprises generating and outputting the sawtooth wave signal, generating and outputting a signal representing the slope of the sawtooth wave signal, where the logic state of the signal representing the sawtooth wave signal changes according to the slope of the sawtooth wave signal, in response to the monitoring signal, generating and outputting the abnormal state detection signal that has different logic states when the monitoring signal is greater than an upper threshold and less than a lower threshold, and generating the switching control signal whose logic state

changes according to the logic state of the abnormal state detection signal and outputting the switching control signal.

According to yet another aspect of the present invention, a class-D amplifier for generating an unsaturated integral signal, comprises: a switching circuit for receiving an integral signal and outputting the integral signal to one of a sub-loop and a steady-state loop; a sub-loop for receiving the integral signal and generating and outputting a first negative feedback signal; a controlled circuit for receiving the integral signal, modulating the integral signal into an output signal, amplifying the output signal, filtering the output signal, and outputting the output signal; and a steady-state loop for receiving the output signal and generating and outputting a second negative feedback signal; wherein the integral signal is unsaturated due to the first and second negative feedback signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The aspects of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

FIG. 1 is a block diagram of a class-D power amplifier according to an exemplary embodiment of the present invention;

FIG. 2 is a block diagram of a feedback control circuit of FIG. 1; and

FIG. 3 is a waveform illustrating an operation of FIGS. 1 and 2 when a fog signal is input.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. 1 is a block diagram of a class-D power amplifier 10 according to an exemplary embodiment of the present invention. Referring to FIG. 1, the class-D power amplifier 10 includes a summing circuit 100, an integral control circuit 200, a feedback control circuit 300, a switching circuit 400, a sub-negative feedback circuit 500, a controlled circuit 600, and a steady-state negative feedback circuit 700.

The summing circuit 100 sums an input signal AIN and a negative feedback signal and outputs an error signal. Here, the input signal AIN is an audio signal and the negative feedback signal is a sub-negative feedback signal output from the

sub-negative feedback circuit 500 or a steady-state negative feedback signal output from the steady-state negative feedback circuit 700, as will be described below. The sub-negative feedback signal or the steady-state negative feedback signal is selected as the negative feedback signal according to a switching control signal D/E output from the feedback control circuit 300.

The integral control circuit 200 outputs an integral signal that is proportionally integrated to the error signal. The feedback control circuit 300 generates and outputs the switching control signal D/E whose logic state changes according to the logic state of an abnormal state detecting signal that is generated in response to a monitoring signal.

FIG. 2 is a block diagram of the feedback control circuit 300 of FIG. 1. Referring to FIG. 2, the feedback control circuit 300 includes a sawtooth wave signal generator 310, a slope detector 320, an abnormal state detector 330, and a feedback decider 340.

The sawtooth wave signal generator 310 generates and outputs a sawtooth wave signal TR1. The sawtooth wave signal TR1 is used in a pulse width modulation (PWM) circuit 610 of the controlled circuit 600. The slope detector 320 generates a signal STR1 representing the slope of the sawtooth wave signal TR1, where the logic state of the sawtooth wave slope representing signal STR1 changes as the slope of the sawtooth wave signal TR1 changes from positive to negative and vice versa.

In response to the monitoring signal, the abnormal state detector 330 generates and outputs an abnormal state detection signal that has different logic states when the monitoring signal is greater than a predetermined upper threshold value and less than a predetermined lower threshold value. Here, the predetermined threshold values are set to be suitable for the desired monitoring capabilities of the class-D power amplifier 10. Thus, the monitoring signal is typically greater than the set predetermined upper threshold value in an abnormal state such as the initial state, an over-current condition, or a power-failure state. The monitoring signal is used to monitor a state in which high power is supplied to the load side such as the speaker, i.e., an abnormal state. The monitoring signal may be an output signal AOUT, a modulated signal of the output signal AOUT, or a signal of part of the controlled circuit 600.

The feedback decider 340 generates and outputs the switching control signal D/E whose logic state changes according to the logic state of the abnormal state detection signal. Here, when the output direction of the integral signal changes from a

sub-loop to a steady-state loop, the logic state of the switching control signal D/E changes in synchronization with the signal STR1, as shown in FIG. 3.

In FIG. 1, the switching circuit 400 receives an integral signal and outputs the integral signal to the sub-loop (i.e., the sub-negative feedback circuit 500) or to the steady-state loop (i.e., the steady-state negative feedback circuit 700) by performing a switching operation corresponding to the logic state of the switching control signal D/E.

The sub-negative feedback circuit 500 processes the integral signal output to the sub-loop and generates and outputs a sub-negative feedback signal as the negative feedback signal. A sub-negative feedback signal generated in an abnormal state prevents the integral signal from becoming saturated.

The controlled circuit 600 modulates the integral signal output to the steady-state loop into a PWM signal PWMO, generates an output signal AOUT using switching amplification and low-pass filtering according to the PWM signal PWMO, and outputs signal AOUT.

As shown in FIG. 1, the controlled circuit 600 includes a PWM circuit 610, a switching amplification circuit 620, and a low-pass filter (LPF) circuit 630. The PWM circuit 610 modulates the integral signal output to the steady-state loop into a PWM signal PWMO using the sawtooth wave signal TR1. After the logic state of the switching control signal D/E changes when the output direction of the integral signal is switched from the sub-loop to the steady-state loop, the PWM signal PWMO maintains a pulse width (indicated by B in FIG. 3) that is half the pulse width of the PWM signal PWMO in the steady-state when the input signal AIN is a fog signal. Here, the PWM signal PWMO has the same pulse width (logic high in FIG. 3) as the switching control signal D/E when the output direction of the integral signal is switched from the sub-loop to the steady-state loop. The fog signal of the input signal AIN is the signal that has no audio signal.

The switching amplification circuit 620 outputs an amplified signal by the switching operation of the switching circuit 400 according to the PWM signal PWMO. The switching amplification circuit 620 outputs the amplified signal by switching operations of a push-up switch and a pull-down switch in response to the PWM signal PWMO.

The LPF circuit 630 outputs an output signal AOUT after low-pass filtering the amplified signal. Low-pass filtering indicates integrating an input digital signal or

converting the input digital signal into an analog signal. The output signal AOUT is output to the load side, such as a speaker, and converted to sound.

In FIG. 1, the steady-state negative feedback circuit 700 processes the output signal AOUT and generates and outputs a steady-state feedback signal as the negative feedback signal.

As pointed out above, the class-D power amplifier 10 includes a switching circuit 400 that receives the integral signal and outputs the integral signal to the sub-loop or to the steady-state loop and the sub-negative feedback circuit 500 that processes the integral signal output to the sub-loop, generates a negative feedback signal, and outputs a sub-negative feedback signal. Consequently, the integral signal is not saturated due to the sub-negative feedback signal generated in an abnormal state.

As described above, the class-D power amplifier 10 prevents the integral control circuit or proportional integral control circuit from becoming saturated by sub-negative feedback loop operations, without using a high-capacity output blocking switch in an initial state or abnormal state. Therefore, it is possible to suppress pop noise due to excessive response characteristics caused when the class-D power amplifier 10 returns to a steady state from an initial state or an abnormal state. In addition, power consumption can be reduced when compared with a conventional power amplifier that uses the output-blocking switch.

As the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and their equivalents.